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(54) Title PHASE SYNCHRONIZATION CIRCUIT

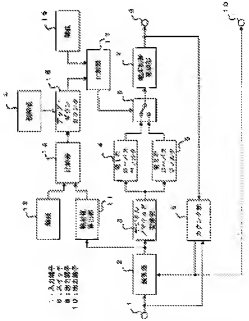
(57) Abstract

Problem

To obtain a phase synchronization circuit that can suppress phase fluctuation, prevent abrupt changes in clock signals, and perform a stable decoding operation, even when signals are input in which phase fluctuation (jitter) has been produced in the clock used by the decoder

Means to solve

In a phase synchronization circuit that provides synchronization processing for clock signals based on differential values between the phase of the aforementioned clock signals used by the decoder and the phase of the reference time information included in the input signal, there are provided a decision means 11-17 that determines whether the aforementioned input signal is a signal in which fluctuation has been produced in the aforementioned clock signal, and a change means 4-6 that changes the response sensitivity of the synchronization processing based on the determination results of the aforementioned decision means.



[See end of patent for translation of figure.]

Claims

1. In a phase synchronization circuit that provides synchronization processing for clock signals based on differential values between the phase of the aforementioned clock signals used by the decoder and the phase of the reference time information included in the input signal,

the phase synchronization circuit is characterized in being provided with: a decision means that determines whether the aforementioned input signal is a signal in which fluctuation has been produced in the aforementioned clock signal,

and a change means that changes the response sensitivity of the synchronization processing based on the determination results of the aforementioned decision means.

2. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned change means makes the response sensitivity of the synchronization processing lower than a prescribed value when the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals.

3. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signal, when the period during which the absolute value of the aforementioned differential value is larger than a certain threshold value continues longer than a prescribed period, or when the probability that the aforementioned absolute value will be larger than a certain threshold value is greater than a prescribed value.

4. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means is provided with: an absolute value calculating unit that calculates the absolute value of the aforementioned differential value, an up–down counter that compares the calculated differential absolute value with a first threshold value and counts upward when it is larger than the first threshold value and counts downward when it is smaller, and a comparator that compares the count value of the aforementioned up–down counter with a second threshold value, and that determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clocks when it is larger than the second threshold value, and determines that the aforementioned signal is not a signal in which fluctuation has been produced in the phase of the aforementioned clocks when it is smaller.

5. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means is provided with: an absolute value calculating unit that calculates the absolute value of the aforementioned differential value, a smoothing unit that provides smoothing processing by collecting a prescribed number of calculated differential absolute values, and a control signal generating unit that determines the degree to which fluctuation has been produced in the phase of the aforementioned clock signals by the

aforementioned input signal according to the magnitude of the output of the aforementioned smoothing unit, and that generates a control signal according to the determination result.

6. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means uses data that represent the validity/invalidity of the input signal as input and determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals, when the period during which invalid data are input continues longer than a prescribed period, or when the probability that invalid data will be input is greater than a prescribed value.

7. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means is provided with: an up–down counter that uses data that represent the validity/invalidity of the input signal as input to find the period during which invalid data are input, that compares the period found with a first threshold value, and that counts upward each time invalid data are input when it is larger than the first threshold value, and counts down when it is smaller, and a comparator that compares the count value of the aforementioned up–down counter, and that determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals when it is larger than the second threshold value, and determines that the aforementioned signal is not a signal in which fluctuation has been produced in the phase of the aforementioned clock signals when it is smaller.

8. The phase synchronization circuit described in Claim 1, characterized in that the aforementioned decision means is provided with: a smoothing unit that uses data that represent the validity/invalidity of the input signal as input and that provides smoothing processing by collecting a prescribed number of periods during which invalid data are input, and a control signal generating means that determines the degree to which fluctuation has been produced in the phase of the aforementioned clock signals by the aforementioned input signal according to the magnitude of the output of the aforementioned smoothing unit, and that generates a control signal according to the determination result.

9. The phase synchronization circuit described in Claim 1, characterized in that changing of the response sensitivity in the aforementioned change means is accomplished by changing the passband of the low pass filter used for synchronization processing.

10. The phase synchronization circuit described in Claim 1, characterized in that changing of the response sensitivity in the aforementioned change means is accomplished by changing the multiplication coefficient of the coefficient unit used for synchronization processing.

11. The phase synchronization circuit described in Claim 1, characterized in being provided with: a smoothing unit that uses data that represent the validity/invalidity of the input

signal as input and that provides smoothing processing by collecting a prescribed number of periods during which invalid data are input, an amount-of-time-shift calculating unit that calculates the amount of time shift in the aforementioned clock signals based on the output of the aforementioned smoothing unit, and a correcting means that corrects the aforementioned clock signals based on the amount of time shift calculated.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention relates to a phase synchronization circuit used in an MPEG decoder or the like for demodulating a program stream or transport stream compressed with the MPEG standard and used in digital broadcasting using satellite broadcasting or terrestrial broadcasting, in cable TV (termed CATV hereafter) that uses a cable, or in a DVD.

[0002]

Prior art

Figure 10 is a block diagram of a digital satellite broadcast receiver using a conventional MPEG decoder that is ordinarily used. In the figure, 101 is an input terminal where the received signal is input, 102 is a tuner module where the received signal is input from input terminal 1, 103 is a descrambler that uses the output from tuner module 102 as input, 104 is an MPEG demultiplexer that uses the output from descrambler 103 as input, 105 is an MPEG video decoder that uses the output from MPEG demultiplexer 104 as input, 106 is an MPEG audio decoder that uses the output from MPEG demultiplexer 104 as input, 107 is an NTSC encoder that uses the output from MPEG video decoder 105 as input, 108 is an output terminal where the NTSC signal is output, 109 is a D/A converter that uses the output from the MPEG audio decoder [105] as input, 110 is an output terminal where the analog audio signal is output, and 111 is a control CPU.

[0003]

Signals are processed in the receiver as follows. First, a satellite signal received by a satellite broadcast receiving antenna is input from input terminal 101 to tuner module 102. Tuner module 102 performs decoding, e.g., switches the received transport stream, demodulates, and corrects errors, and extracts an MPEG transport stream in which individual data strings (streams) are multiplexed. The transport stream (termed TS hereafter) is input to descrambler 103 and is decrypted, and is transferred to MPEG demultiplexer 104. MPEG demultiplexer 104 receives the program specification information (termed PSI hereafter) based on the viewer tuning operation,

extracts the necessary video data and audio data from the TS, and outputs them to MPEG video decoder 105 and MPEG audio decoder 106. MPEG video decoder 105 decompresses the video data, they are converted to an NTSC signal by NTSC encoder 107 and the NTSC signal is output to the TV receiver from output terminal 108. MPEG audio decoder 106 decompresses the audio data, and they are converted to an analog audio signal by D/A converter 109 and are output to the TV receiver from output terminal 110. Control CPU 111 controls this processing sequence.

[0004]

Note that with CATV, too, digital signals received via cable undergo the same processing as described above and are output to the TV receiver. Thus MPEG demultiplexer 104 has the function of separating the MPEG TS included in the received satellite signal into video data, audio data, and other control data. At the same time, it also has the function of providing reproduction processing for the clock signal used by MPEG demultiplexer 104, MPEG video decoder 105, MPEG audio decoder 106, and NTSC encoder 107.

[0005]

The clock signal reproduction process is common time management, that is, processing to achieve synchronization between the MPEG encoder (encoding device) that encodes and compresses the video data or audio data at the broadcaster side and the MPEG decoder (decoding device) that decompresses the video data or audio data at the viewer side. Next, the clock signal reproduction processing is explained.

[0006]

Figure 11 is a block diagram that shows the configuration of a phase synchronization circuit used for clock signal reproduction processing. In the figure, 1 is an input terminal where the TS signal is input, 2 is a subtracting unit (phase comparison unit) that subtracts the value of a synchronization signal, as time reference (System Time Clock: termed STC hereafter) in the MPEG decoder, that is output from a counter unit 9, described below, from a program time reference value (Program Clock Reference: termed PCR hereafter) that is included in the TS signal input from input terminal 1, 3 is a digital/analog converting unit (termed D/A converting unit hereafter) that converts the digital signal output by subtracting unit 2 to an analog signal, 4 is a first low pass filter (termed first LPF hereafter) that uses the output of D/A converting unit 3 as input, 7 is a voltage-controlled oscillation unit (Voltage-control Oscillator: termed VCO hereafter) that uses the output of first LPF 4 as input, 8 is an output terminal that outputs a clock to later-stage circuitry, and 9 is a counter unit that counts the clocks output by VCO 7.

[0007]

The PCR extracted and separated from the TS is used for clock signal reproduction processing in the phase synchronization circuit. The PCR is information for setting and correcting the STC value to the value intended by the MPEG broadcaster side, that is, a 27 MHz clock frequency in the case of MPEG 2, in the MPEG decoders, including the video decoder 105 and the audio decoder 106, and it is included at a length of 42 bits in a specific stream. Following, is an explanation of the reproduction processing for clock signal CLK. First, the PCR value extracted from a specific stream is written (set) without change into counter unit 9, and the STC and PCR output from counter unit 9 are initialized as synchronized (same value). Counter 9 uses the written PCR as the initial value and counts upward by counting the received clocks output from VCO 7. When the next PCR is input, subtraction processing with the STC from counter unit 9 when the PCR was received is performed in subtracting unit 2. When the phases of both clock signals for the PCR and STC agree perfectly, the output of the subtracting unit will be 0. On the other hand, when the two phases differ, the difference is converted to a voltage signal via D/A converting unit 3 and first LPF 4 and is applied to VCO 7. The phase of CLK is corrected due to the frequency of the clock signal CLK output from VCO 7 being corrected by the voltage signal. Counter unit 9 is configured to count upward according to the clock signal CLK output from VCO 7, so the count value, that is, the phase of the STC, is controlled according to the change in output from VCO 7.

[0008]

The phase of the clock signal CLK on the MPEG decoder side can be accurately matched to that of the MPEG encoder side by processing to reproduce the clock signal based on the PCR in this way. It is therefore possible to prevent an overflow or underflow state in the amount of data in the buffer memories provided ancillary to video decoder 105 and audio decoder 106, and it is possible to achieve synchronization between the video data and audio data in the reproduced output that use time management information (Presentation Time Stamp: termed PTS hereafter). The clock signal reproduction processing by such a phase synchronization circuit is premised on the PCR in the stream having been generated accurately.

[0009]

Problems to be solved by the invention

Incidentally, the structure of a packet in which many individual streams are time-division-multiplexed (transport stream packet: termed TS packet hereafter) has a multiple-level structure included [sic; composed] from the packet elementary stream (Packetized Elementary

Stream: termed PES hereafter) packets that include the video elementary stream and the audio elementary stream, and PSI, PCR, etc., in different levels from the PES packets.

[0010]

At the MPEG encoder side, therefore, when TS packets are generated directly from input data, creating and inserting a PCR can be easily accomplished, but to synthesize only elementary stream or PES packet data and generate a TS packet, because the PCR is included in the TS packet level, the phase of the clock at the time the elementary stream is created is not reflected, and it is not possible to create and insert an accurate PCR.

[0011]

In addition, in cases such as when, because of the communication network relationship, transmission is through a communication network that transmits with the transmission speed increased in order to transmit by multiplexing with other information in time division, at the transmitting side, time is read at random intervals from a counter that counts based on the reference frequency from a transmission reference clock source, and it is transmitted to the communication network as time information PCR.

[0012]

The time information PCR is read from the counter at random intervals within a prescribed interval of 100 ms, so this value represents time T from the reading immediately prior. At the receiving side, the time information is received via the aforementioned communication network as reception time information, and a reception clock is reproduced by a phase synchronization circuit. When the transmission signal in this case is transmitted with the transmission speed increased, the TS data are temporally compressed along with a valid data period signal into a period indicated by the aforementioned valid data period signal, and are transmitted in bursts. Time shift occurs in the time information, and the arrival time of the reception time information fluctuates. In addition, the above was explained for TS, but the same occurs in a program stream as well. In the case of the aforementioned program stream, the system time reference value (System Clock Reference: termed SCR hereafter) is read from the counter in the same way at random intervals within a prescribed interval of 700 ms, so this value represents time T from the reading immediately prior. At the receiving side, time information is received via the aforementioned communication network as reception time information, and a reception clock is reproduced by a phase synchronization circuit.

[0013]

Fluctuation in the arrival time of the time information as described above appears as fluctuation (jitter) in the phase of the STC. This type of phase fluctuation cannot be controlled with a conventional phase synchronization circuit, so there is the problem that stable reception operation is not possible for the transmission signal from a communication network as described above.

[0014]

With solutions for the problem as described above, for example, with H.220.0 as recommended by ITUT-T, a method is disclosed to buffer the received data, and use the transmission rate indicated in the syntax of the received data to transmit at an approximately constant rate from the buffer. The aforementioned transmission rate does not necessarily indicate an accurate rate, though, so that in addition to adding a buffer, there is the problem that data sufficiency in the buffer must be monitored and controlled.

[0015]

The present invention was devised to solve the problems described above, and the objective is to provide a phase synchronization circuit that can prevent overflow or underflow in the amount of data in the buffer memories provided ancillary to video decoder 105, and audio decoder 106, and that can achieve synchronization between video data and audio data in reproduction outputs that use PTS, by reproducing clocks precisely, even when fluctuation occurs in the phase near the sampling frequency.

[0016]

Means to solve the problems

The phase synchronization circuit pertaining to the present invention is characterized in that, in a phase synchronization circuit that provides synchronization processing for clock signals based on differential values between the phase of the aforementioned clock signals used by the decoder and the phase of the reference time information included in the input signal, there are provided a decision means that determines whether the aforementioned input signal is a signal in which fluctuation has been produced in the aforementioned clock signal, and a change means that changes the response sensitivity of the synchronization processing based on the determination results of the aforementioned decision means.

[0017]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned change means is configured to change the response sensitivity of the synchronization processing when the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals.

[0018]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned decision means is configured to determine that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals when the period during which the absolute value of the aforementioned differential value is larger than a certain threshold value continues longer than a prescribed period, or when the probability that the aforementioned absolute value will be larger than a certain threshold value is greater than a prescribed value.

[0019]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned decision means is configured from: an absolute value calculating unit that calculates the absolute value of the aforementioned differential value, an up–down counter that compares the calculated differential absolute value with a first threshold value and counts upward when it is larger than the first threshold value and counts downward when it is smaller, and a comparator that compares the count value of the aforementioned up–down counter with a second threshold value, and that determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clocks when it is larger than the second threshold value, and determines that the aforementioned signal is not a signal in which fluctuation has been produced in the phase of the aforementioned clocks when it is smaller.

[0020]

The phase synchronization circuit pertaining to the present invention is characterized in that the aforementioned decision means is configured from: an absolute value calculating unit that calculates the absolute value of the aforementioned differential value, a smoothing unit that provides smoothing processing by collecting a prescribed number of calculated differential absolute values, and a control signal generating unit that determines the degree to which fluctuation has been produced in the phase of the aforementioned clock signals by the aforementioned input signal according to the magnitude of the output of the aforementioned smoothing unit, and that generates a control signal according to the determination result.

[0021]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned decision means is configured so as to use data that represent the validity/invalidity of the input signal as input and to determine that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals, when the period during which invalid data are input continues longer than a prescribed period, or when the probability that invalid data will be input is greater than a prescribed value.

[0022]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned decision means is configured from: an up–down counter that uses data that represent the validity/invalidity of the input signal as input to find the period during which invalid data are input, that compares the period found with a first threshold value, and that counts upward each time invalid data are input when they are larger than the first threshold value, and counts downward when they are smaller, and a comparator that compares the count value of the aforementioned up–down counter with a second threshold value, and that determines that the aforementioned input signal is a signal in which fluctuation has been produced in the phase of the aforementioned clock signals when it is larger than the second threshold value, and determines that the aforementioned signal is not a signal in which fluctuation has been produced in the phase of the aforementioned clock signals when it is smaller.

[0023]

The phase synchronization circuit pertaining to the present invention is also characterized in that the aforementioned decision means is configured from: a smoothing unit that uses data that represent the validity/invalidity of the input signal as input and that provides smoothing processing by collecting a prescribed number of periods during which invalid data are input, and a control signal generating means that determines the degree to which fluctuation has been produced in the phase of the aforementioned clock signals by the aforementioned input signal according to the magnitude of the output of the aforementioned smoothing unit, and that generates a control signal according to the determination result.

[0024]

The phase synchronization circuit pertaining to the present invention is also characterized in being configured so that the changing of the response sensitivity in the aforementioned change

means is accomplished by changing the passband of the low pass filter used for the synchronization processing.

[0025]

The phase synchronization circuit pertaining to the present invention is also characterized in being configured so that the changing of the response sensitivity in the aforementioned change means is accomplished by changing the multiplication coefficient of the coefficient unit used for the synchronization processing.

[0026]

The phase synchronization circuit pertaining to the present invention is also characterized in being configured to be additionally provided with: a smoothing unit that uses data that represent the validity/invalidity of the input signal as input and that provides smoothing processing by collecting a prescribed number of periods during which invalid data are input, an amount-of-time-shift calculating unit that calculates the amount of time shift in the aforementioned clock signals based on the output of the aforementioned smoothing unit, and a correcting means that corrects the aforementioned clock signals based on the amount of time shift calculated.

[0027]

Embodiments of the invention

The present invention is explained concretely below based on figures that show embodiments thereof.

Embodiment 1

Figure 1 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 1 of the present invention. In the figure, 1 is an input terminal where the PCR included in the TS is input, 2 is a subtracting unit that subtracts the STC output from counter unit 9, described below, from the PCR that is input, 3 is a D/A converter that converts the digital signal value output by subtracting unit 2 to an analog signal, 4 is a first LPF that uses the output of D/A converting unit 3 as input, 5 is a second LPF that uses the output of D/A converting unit 3 as input, 6 is a switch unit that switches between—and outputs—the output of first LPF 4 and the output of second LPF 5 based on the output of a comparator 17, described below, and the response sensitivity of the phase synchronization circuit is changed by said switch unit. 7 is a VCO that uses the output of switch unit 6 as input, 8 is an output terminal where the received clock output from the VCO is output, 9 is a counter unit that counts the received clocks output

from the VCO, 10 is an output terminal that outputs the STC output from counter unit 9 to a later stage, 11 is an absolute value calculating unit that uses the digital signal value output from subtractor [sic] 2 as input, 12 is a threshold value that represents an arbitrary value, 13 is a comparator that uses the output of absolute value calculating unit 11 and threshold value 12 as input, 14 is the initial value of an up–down counter 15, described below, 15 is an up–down counter that uses the output of comparator 13 and initial value 14 as input, 16 is a threshold value that represents an arbitrary value, and 17 is a comparator that uses the output of up–down counter 15 and threshold value 16 as input. A decision means is configured by absolute value calculating unit 11 through comparator 17.

[0028]

Subtracting unit 2 provides subtraction processing for the PCR input from input terminal 1 and the STC output from counter unit 9. When the phases of the clock signals for both the PCR and STC agree perfectly, the output from subtracting unit 2 will be 0. On the other hand, when the two phases do not agree, the differential value is output to D/A converting unit 3 and absolute value calculating unit 11. The output from D/A converting unit 3 is converted to a voltage signal through either first LPF 4 or second LPF 5, with different characteristics, that are switched by switch unit 6 according to a decision signal from the decision means, and is applied to VCO 7. VCO 7 corrects the phase, due to the frequency of the received clock being corrected by the aforementioned voltage signal, and outputs it to output terminal 8. Counter unit 9 is configured to count up the received clocks output from VCO 7, so the count value, that is, the phase of the STC, is controlled according to changes in the output from VCO 7.

[0029]

Absolute value calculating unit 11 calculates the absolute value of the differential value output from subtracting unit 2. When the absolute value of the differential value is larger than arbitrary threshold value 12 according to comparator 13, up–down counter 15 is caused to count upward each time a PCR arrives, and to count downward when it is smaller. Comparator 17 switches switch unit 6 so that the voltage signal is passed through first LPF 4, the same as in the conventional example, when the count value of up–down counter 15 is smaller than arbitrary threshold value 16, and switches switch unit 6 so that the voltage signal is passed through second LPF 5, which passes only bands lower than first LPF 4, when it is larger. Note that up–down counter 15 sets an initial value each time the phase synchronization circuit to which a new TS is input starts synchronization processing.

[0030]

With the operation above, when time shift occurs in the PCR arrival time due to the fact that TS data are time-compressed by transmission signal processing and are transmitted in bursts and the probability that the absolute value of the differential value between the aforementioned PCR and the MPEG decoder STS will be calculated to be larger than arbitrary threshold value 12 increases, the value in up–down counter counter [sic] 15 will become larger. When this value is larger than arbitrary threshold value 16, the decision means determines that TS data in which STC phase fluctuation (jitter) has been produced have been input, and it switches the LPF, which is the loop portal to the phase synchronization circuit, to second LPF 5 with lower sensitivity. Synchronization processing with low-sensitivity response is thereby performed and phase fluctuation can be suppressed.

[0031]

Embodiment 2.

Figure 2 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 2 of the present invention. In the figure, 18 is an input terminal that receives input of a valid data synchronization signal that indicates the period during the input TS signal during which valid data are input, 19 is a counter unit that where the valid data period signal that is input from input terminal 18 is input, 20 is a threshold value that represents an arbitrary value, 21 is a comparator that uses the output from counter unit 19 and threshold value 20 as input, 22 is a threshold value that represents an arbitrary value, 22 is the initial value for up–down counter 23, described below, 23 is an up–down counter that uses the output from comparator 21 and initial value 22 as input, 24 is a threshold value that represents an arbitrary [value], and 25 is a comparator that uses the output from up–down counter 23 and threshold value 24 as input. A decision means is configured from counter unit 19 to comparator 25.

[0032]

Counter unit 19 uses the valid data period signal, which indicates the period within the TS signal input from input terminal 18 during which valid data are input, to count received clock using the point at which invalid data start to be input as the starting point, and converts the width of the invalid period into a numerical value as the received clock count value. The invalid period width converted to a numerical value is compared with arbitrary threshold value 20 by comparator 21, and when the invalid period width converted to a numerical value is larger, up–down counter 23 is caused to count upward each time invalid data are input, and to count downward when it is smaller. Comparator 25 switches switch unit 6 so that the voltage signal will pass through first LPF 4, the same way as in the conventional example, when the count

value of up–down counter 23 is smaller than arbitrary threshold value 24, and switches switch unit 6 so that the voltage signal will pass through second LPF 5, which passes only bands lower than first LPF 4, when it is larger. Note that up–down counter 23 sets an initial value each time the phase synchronization circuit to which a TS is input starts synchronization processing.

[0033]

With the above processing, when a signal is input such that time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts, when the frequency of arrival of an invalid period width at a width greater than arbitrary threshold value 20 increases, using the valid data period signal that indicates the period within the TS signal during which valid data are input, counter 23 value of the up–down counter becomes larger. When this value is larger than arbitrary threshold value 24, the decision means determines that TS data in which fluctuation (jitter) in the STC phase has been produced have been input, and it switches the LPS, which is the loop filter for the phase synchronization input, to second LPF 5 with low sensitivity. Synchronization processing with low-sensitivity response is thereby performed and phase fluctuation can be suppressed.

[0034]

Embodiment 3

Figure 3 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 3 of the present invention. In the figure, 26 is a first coefficient unit where the output from subtractor 2 is input, 27 is a second coefficient unit where the output from subtractor 2 is input, and 28 is a selector that switches between the output from first coefficient unit 26 and the output from second coefficient unit 27 based on the output from comparator 17, and the response sensitivity of the phase synchronization circuit is changed by said selector. 29 is an adder that uses the output from selector 28 and the output from a D flip-flop, described below, as input, and 30 is a D flip-flop that uses the output from adder 29 as input. The decision means is the same as that explained with embodiment 1.

[0035]

First coefficient unit 26 multiplies the differential value from subtractor 2 by coefficient A in $0 < A < 1$, and second coefficient unit 27 multiplies it by coefficient B in $0 < B < A < 1$. Selector 28 selects the differential value multiplied by the first coefficient unit when the count value of up–down counter 15 is smaller than arbitrary threshold value 16, and selects the differential value multiplied by the second coefficient unit when it is larger. Adder 29 adds the differential value multiplied by either one of the coefficients and the digital value of the control

voltage output from D flip-flop 30, described below. D flip-flop 30 stores the digital value of the control voltage output from adder 29 at the timing of each time a PCR is input. D/A converting unit 3 converts the value stored by the D flip-flop to a voltage signal and applies it to VCO 7.

[0036]

With the operation above, when time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts and the probability of the differential value between the aforementioned PCR and the absolute value of the value of the synchronization signal, which is the MPEG decoder time standard, being calculated as greater than arbitrary threshold value 12 increases, the counter 15 value of the up–down counter will become larger. When this value is larger than arbitrary threshold value 16, the decision means determines that TS data in which fluctuation (jitter) in the phase of the STC has been produced have been input, and it switches to the second coefficient unit whereby the coefficient unit [sic; coefficient] of the digital recursive-type loop filter configured with first coefficient unit 26, adder 29 and D flip-flop 30 of the phase synchronization circuit is multiplied [sic; multiplies] with a smaller coefficient. Synchronization processing with low-sensitivity response is thereby performed and phase fluctuation can be suppressed.

[0037]

Embodiment 4

Figure 4 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 4 of the present invention. In the figure, 28 is a selector that switches between the output from first coefficient unit 26 and the output from second coefficient unit 27 based on the output from comparator 25, and the response sensitivity of the phase synchronization circuit is changed by said selector. The decision means is the same as in embodiment 2.

[0038]

Selector 28 selects the differential value multiplied by the first coefficient unit when the count value of up–down counter 23 is smaller than arbitrary threshold value 24, and selects the differential value multiplied by the second coefficient unit when it is larger.

[0039]

With the operation above, when a signal in which time shift will occur in the PCR arrival time due to the TS dating being time-compressed and transmitted in bursts, when the frequency of arrival of the invalid period width at a width greater than arbitrary threshold value 20 becomes greater using the valid data period signal that indicates the period within the TS signal during

which valid data are input, and the value 23 counter of the up–down counter becomes larger and the value is larger than arbitrary threshold value 24, the decision unit determines that TS data in which fluctuation (jitter) in the phase of the STC has been produced have been input, and it switches to the second coefficient whereby the coefficient unit [sic; coefficient] of the digital recursive-type loop filter configured with first coefficient unit 26, adder 29 and D flip-flop 30 of the phase synchronization circuit is multiplied [sic; multiplies] with a smaller coefficient. Synchronization processing with low-sensitivity response is thereby performed and phase fluctuation can be suppressed.

[0040]

Embodiment 5

Figure 5 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 5 of the present invention. In the figure, 31 is a smoothing unit that uses the output from absolute value calculating unit 11 as input, 32 is a control signal generating unit that uses the output from smoothing unit 31 as input, and 33 is a variable coefficient unit that changes the coefficient for multiplying the output from subtractor 2 based on the output from control signal generating unit 32, and the response speed of the phase synchronization circuit is changed by said variable coefficient unit. 29 is an adder that adds the output from variable coefficient unit 33 and [the output from] D flip-flop 30. The decision means is configured by absolute value calculating unit 11, smoothing unit 31, and control signal generating unit 32.

[0041]

Variable coefficient unit 33 multiplies the differential value from subtractor 2 by coefficient X in $0 < X < 1$. Coefficient X is selected in stages by a control signal output from control signal generating unit 32, described below. Adder 29 adds the differential value that has been multiplied by the variable coefficient unit and the digital value of the control voltage output from D flip-flop 30, described below. D flip-flop 30 stores the digital value of the control voltage output from adder 29 at the timing of each time a PCR is input. D/A converting unit 3 converts the value stored by the D flip-flop to a voltage signal and applies it to VCO 7.

[0042]

Absolute value calculating unit 11 calculates the absolute value of the differential value output from aforementioned subtracting unit 2, and the absolute value of the differential value that is calculated an arbitrary number of times is smoothed by smoothing unit 31. Control signal generating unit 32 generates a control signal according to the value output from smoothing unit

31. Variable coefficient unit 33 switches the coefficient in stages so that coefficient X will become smaller, the larger the value output from smoothing unit 31.

[0043]

With the operation above, time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts, the differential value between the aforementioned PCR and the STC, which is the value of the synchronization signal that is the MPEG decoder time standard, is calculated, and the absolute value of the differential value is smoothed an arbitrary number of times. When this value becomes larger, the decision means determines that TS data in which fluctuation (jitter) has been produced in the phase of the STC have been input, and it switches the coefficient of the digital recursive-type loop filter configured with multistage [sic; variable] coefficient unit 33, adder 29 and D flip-flop 30 of the phase synchronization circuit according to the value so that multiplication is performed by using the switched coefficient. The phase synchronization circuit can thereby accomplish more precise synchronization processing with low-sensitivity response according to the state of the TS data, and phase fluctuation is suppressed. Note that with this embodiment, a case in which the multiplication coefficient for variable coefficient unit 33 is switched based on the output from control signal generating unit 32 was explained, but the phase synchronization circuit could also be configured as in embodiment 1, and it could be configured so that the passband of the LPF is switched and controlled.

[0044]

Embodiment 6

Figure 6 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 6 of the present invention. In the figure, 34 is a smoothing unit that uses the output from counter unit 19 as input, 35 is a control signal generating unit that uses the output from smoothing unit 34 as input, 33 is a variable coefficient unit that changes the coefficient for multiplying the output from subtractor 2 based on the output from control signal generating unit 35, and the response speed of the phase synchronization circuit is changed by said variable coefficient unit. A decision unit is constituted by counter unit 19, smoothing unit 34 and control signal generating unit 35.

[0045]

Smoothing unit 34 uses a valid data period signal, which indicates the period within the TS signal counted by counter unit 19 during which valid data are input, counts the received clocks using the point at which invalid data start to be input as the starting point, smoothes the

invalid period width converted to a numerical value in an arbitrary number of times that invalid data arrive. Control signal generating unit 35 generates a control signal according to the value output from smoothing unit 34. Variable coefficient unit 33 switches the coefficient in stages so that coefficient X will become smaller, the larger the value output from smoothing unit 35 [sic; 34].

[0046]

With the operation above, when a signal is input such as when time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts, the valid data period signal, which indicates the period within the TS signal during which valid data are input, is used, and a prescribed number of invalid period widths are collected and smoothed. Then, when this value becomes larger, the decision unit determines that TS data in which fluctuation (jitter) has been produced in the phase of the STC have been input, the coefficient of the digital recursive-type loop filter configured with variable coefficient unit 33, adder 29, and D flip-flop 30 of the phase synchronization circuit is switched in stages according to that value, and multiplication is performed using the switched coefficient. The phase synchronization circuit can thereby accomplish more precise synchronization processing with low-sensitivity response according to the state of the TS data, and phase fluctuation is suppressed. Note that with this embodiment, a case in which the multiplication coefficient for variable coefficient unit 33 is switched based on the output from control signal generating unit 35 was explained, but the phase synchronization circuit could also be configured as in embodiment 2, and it could be configured so that the LPF passband is switched and controlled.

[0047]

Embodiment 7

Figure 7 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 7 of the present invention. In the figure, 34 is a smoothing unit that uses the output from counter unit 19 as input, 36 is an amount-of-time-shift calculating unit that uses the output from smoothing unit 34 as input, 37 is an adder that uses the STC, as the output from counter unit 9, and the output from amount-of-time-shift calculating unit 36 as input, and 10 is an output terminal that outputs the corrected STC output from adder 37 to a later stage. The configuration other than smoothing unit 34, amount-of-time-shift calculating unit 36 and adder 37 is the same as embodiment 2, so a detailed explanation will be omitted.

[0048]

Smoothing unit 34 uses the valid data period signal, which indicates the period within the TS signal counted by counter unit 19 during which valid data are input, counts the received clocks using the point at which invalid data start to be input as the starting point, and smoothes the invalid period width converted to a numerical value by an arbitrary number of times that invalid data arrive. Amount-of-time-shift calculating unit 36 calculates time shift in the PCR arrival time produced due to the TS data being time-compressed and transmitted in bursts from the invalid period width converted to a numerical value and output from smoothing unit 34, and converts the time shift to a received clock count value and outputs it. Adder 37 adds the STC output from counter 9 and the time shift converted to received clock value output from amount-of-time-shift calculating unit 36, and functions as a correcting means that outputs this as corrected STC to a later stage.

[0049]

With the operation above, when a signal is input such as when time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts, when there is an increase in the frequency at which an invalid period width arrives at a width larger than fixed threshold value 20, the counter 23 value of the up–down counter increases, using the valid data period signal that indicates the period within the TS signal during which valid data are input. When this value is larger than arbitrary threshold value 24, the decision means determines that TS data in which fluctuation (jitter) has been produced in the phase of the STC have been input and it switches the LPF, which is the loop filter of the phase synchronization circuit, to second LPF 5 that has low sensitivity. In addition, the invalid period width is smoothed by the arbitrary number of times that the invalid data arrive (smoothing unit 34), the amount of time shift in the STC generated by the phase synchronization circuit is calculated based on this value (amount-of-time-shift calculating unit 36), and the corrected value is added in adder 37. With these operations, the phase synchronization circuit can carry out synchronization processing with low-sensitivity response, phase fluctuation can be suppressed, time shift in the STC generated by the phase synchronization circuit can be corrected, and MPEG processing can be accomplished.

[0050]

Embodiment 8

Figure 8 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 8 of the present invention. As is clear from the figure, the configuration, except for smoothing unit 34, amount-of-time-shift calculating unit 36, and adder 37, is the same as Figure 4 explained in embodiment 4.

[0051]

The operation is the same as that explained with embodiments 4 and 7 described above, and is explained briefly below. When a signal such as when time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts is input, when there is an increase in the frequency at which an invalid period width arrives at a width larger than fixed threshold value 20, the counter 23 value of the up–down counter increases using the valid data period signal that indicates the period within the TS signal during which valid data are input. When this value is larger than arbitrary threshold value 24, the decision means determines that TS data in which fluctuation (jitter) has been produced in the phase of the STC have been input and it switches to the second coefficient unit whereby the coefficient unit [sic; coefficient] of the digital recursive-type loop filter configured with first coefficient unit 26, adder 29, and D flip-flop 30 of the phase synchronization circuit is multiplied with a smaller coefficient. In addition, the invalid period width is smoothed by the arbitrary number of times that invalid data arrive, the amount of time shift in the STC generated by the phase synchronization circuit is corrected based on this value, and the corrected value is added in adder 37. With these operations, the phase synchronization circuit can carry out synchronization processing with low-sensitivity response, phase fluctuation can be suppressed, time shift in the STC generated by the phase synchronization circuit can be corrected, and MPEG processing can be accomplished.

[0052]

Embodiment 9

Figure 9 shows a phase synchronization circuit in an MPEG data receiving device that is embodiment 9 of the present invention. As is clear from the figure, the configuration, except for amount-of-time-shift calculating unit 36 and adder 37, is the same as Figure 6 explained in embodiment 6.

[0053]

The operation is the same as that explained with embodiments 6 and 7 described above, and is explained briefly below. When a signal such as when time shift occurs in the PCR arrival time due to the TS data being time-compressed and transmitted in bursts is input, the valid data period signal that indicates the period within the TS data during which valid data are input is used, and a prescribed number of invalid period widths is collected in order to smooth them. Then, when this value becomes larger, the decision means determines that TS data in which fluctuation (jitter) has been produced in the phase of the STC have been input, it switches the coefficient of the digital recursive-type loop filter configured with multi-stage coefficient unit 33,

adder 29, and D flip-flop 30 of the phase synchronization circuit in stages according to the value, and multiplication is carried out using the switched count [sic; coefficient]. In addition, the invalid period width is smoothed by an arbitrary number of times that invalid data arrive, the amount of shift in the STC generated by the phase synchronization circuit is calculated based on that value, and the corrected value is added in adder 37. With these operations, the phase synchronization circuit can carry out synchronization processing with low-sensitivity response according to the state of the TS data that are input, phase fluctuation can be suppressed, time shift in the STC generated by the phase synchronization circuit can be corrected, and MPEG processing can be accomplished.

[0054]

Note that embodiments 1-9 were explained with extraction and processing of the PCR included in the TS signal, using a TS as the input signal, but the same effects are obtained by extracting and processing the SCR included in a program stream where the input signal is a program stream. In addition, aforementioned embodiments 7-9 were explained where a circuit for STC correction (smoothing unit 34, amount-of-time-shift calculating unit [36], adder 37) were provided for the phase synchronization circuits in embodiments 2, 4, and 6, but naturally this could also be provided for the phase synchronization circuits in embodiments 1, 3, and 5. For example, in the phase synchronization circuits in Figure 1, Figure 3, and Figure 5, valid data period signal input terminal 18, counter unit 19, smoothing unit 34, an amount-of-time-shift calculating unit [36], and adder 37 are added, the output from VCO 7 is also input to counter 19, and from subtractor 2 to output terminal 10 would be connected through adder 37.

[0055]

Effects of the invention

The present invention is configured as explained above, and so effects as shown below are achieved.

[0056]

With the phase synchronization circuit pertaining to the present invention, when a signal in which phase fluctuation (jitter) has been produced in the clock used by the decoder is input, the phase synchronization circuit is configured so that the response sensitivity is switched to low sensitivity. Thus, there is the effect that phase fluctuation can be suppressed, abrupt changes in the clock signal can be avoided, and a stable decoding operation can be realized.

[0057]

In addition, with the phase synchronization circuit pertaining to the present invention, time offset included in the clock can be removed, so there is the effect that decoding processing, which in the past would have decoded with a time offset, can become decoding processing with the original time, and accurate synchronization can be achieved in the reproduction of the data.

Brief description of the figures

Figure 1 is a phase synchronization circuit diagram that shows embodiment 1 of the present invention.

Figure 2 is a phase synchronization circuit diagram that shows embodiment 2 of the present invention.

Figure 3 is a phase synchronization circuit diagram that shows embodiment 3 of the present invention.

Figure 4 is a phase synchronization circuit diagram that shows embodiment 4 of the present invention.

Figure 5 is a phase synchronization circuit diagram that shows embodiment 5 of the present invention.

Figure 6 is a phase synchronization circuit diagram that shows embodiment 6 of the present invention.

Figure 7 is a phase synchronization circuit diagram that shows embodiment 7 of the present invention.

Figure 8 is a phase synchronization circuit diagram that shows embodiment 8 of the present invention.

Figure 9 is a phase synchronization circuit diagram that shows embodiment 9 of the present invention.

Figure 10 is a figure that shows a digital satellite broadcast receiver that uses a conventional MPEG decoder.

Figure 11 is a conventional phase synchronization circuit diagram.

Explanation of symbols

1 Input terminal, 2 Subtractor, 3 Digital/analog converter, 4 First low pass filter, 5 Second low pass filter, 6 Switch, 7 Voltage-controlled oscillator unit, 8 Output terminal, 9 Counter unit, 10 Output terminal, 11 Absolute value calculating unit, 12 Threshold value, 13 Comparator, 14 Initial value, 15 Up–down counter, 16 Threshold value, 17 Comparator, 18 Input terminal, 19 Counter unit, 20 Threshold value, 21 Comparator, 22 Initial value, 23 Up–down counter, 24 Threshold value, 25 Comparator, 26 First coefficient unit, 27 Second coefficient unit,

28 Selector, 29 Adder, 30 D flip-flop, 31 Smoothing unit, 32 Control signal generating unit, 33 Variable coefficient unit, 34 Smoothing unit, 35 Control signal generating unit, 36 Amount-of-time-shift calculating unit, 37 Adder, 101 Input terminal, 102 Tuner module, 103 Descrambler, 104 MPEG demultiplexer, 105 MPEG video decoder, 106 MPEG audio decoder, 107 NTSC encoder, 108 Output terminal, 109 D/A converter, 110 Output terminal, 111 Control CPU.

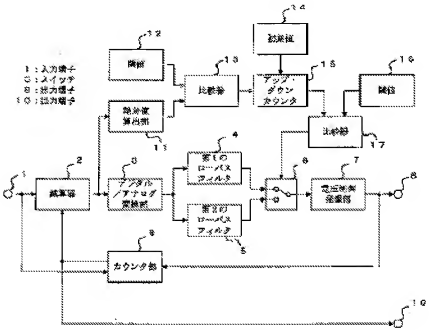


Figure 1

Legend:
1: Input terminal
6: Switch
8: Output terminal
10: Output terminal

Key:
2 Subtractor
3 Digital/analog converting unit
4 First low pass filter
5 Second low pass filter
7 Voltage-controlled oscillation unit
9 Counter unit
11 Absolute value calculating unit
12 Threshold value
13 Comparator
14 Initial value
15 Up–down counter
16 Threshold value
17 Comparator

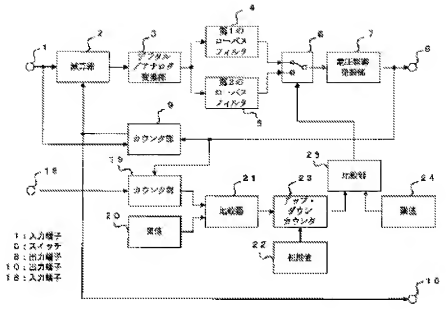


Figure 2

Legend: 1: Input terminal
6: Switch
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
4 First low pass filter
5 Second low pass filter
7 Voltage-controlled oscillation unit
9 Counter unit
19 Counter unit
20 Threshold value
21 Comparator
22 Initial value
23 Up–down counter
24 Threshold value
25 Comparator

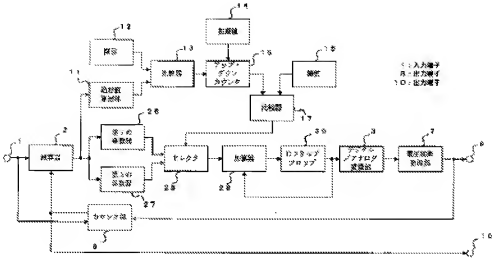


Figure 3

Legend: 1: Input terminal
8: Output terminal
10: Output terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
11 Absolute value calculating unit
12 Threshold value
13 Comparator
14 Initial value
15 Up–down counter
16 Threshold value
17 Comparator
26 First coefficient unit
27 Second coefficient unit
28 Selector
29 Adder
30 D flip-flop

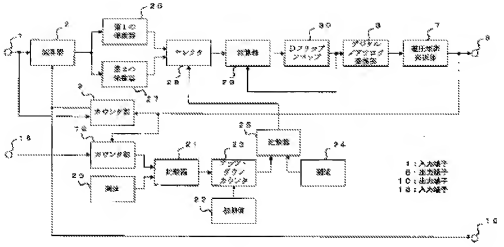


Figure 4

Legend: 1: Input terminal
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
19 Counter unit
20 Threshold value
21 Comparator
22 Initial value
23 Up–down counter
24 Threshold value
25 Comparator
26 First coefficient unit
27 Second coefficient unit
28 Selector
29 Adder
30 D flip-flop

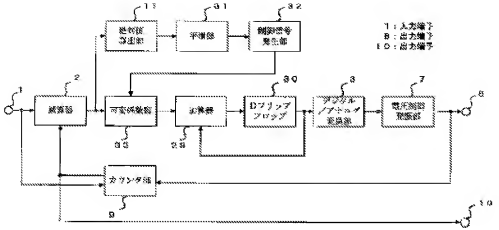


Figure 5

Legend: 1: Input terminal
8: Output terminal
10: Output terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
11 Absolute value calculating unit
29 Adder
30 D flip-flop
31 Smoothing unit
32 Control signal generating unit
33 Variable coefficient unit

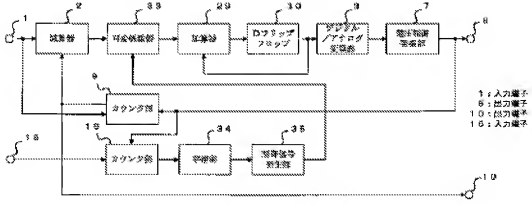


Figure 6

Legend: 1 Input terminal
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
19 Counter unit
29 Adder
30 D flip-flop
33 Variable coefficient unit
34 Smoothing unit
35 Control signal generating unit

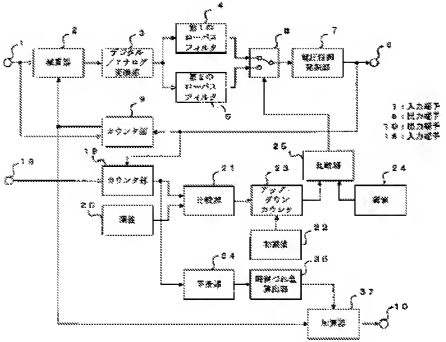


Figure 7

Legend: 1: Input terminal
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
4 First low pass filter
5 Second low pass filter
7 Voltage-controlled oscillation unit

9 Counter unit
19 Counter unit
20 Threshold value
21 Comparator
22 Initial value
23 Up–down counter
24 Threshold value
25 Comparator
34 Smoothing unit
36 Amount-of-time-shift calculating unit
37 Adder

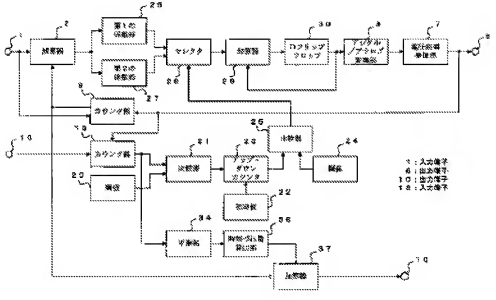


Figure 8

Legend: 1: Input terminal
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
20 Threshold value
21 Comparator
22 Initial value
23 Up–down counter
24 Threshold value
25 Comparator
26 First coefficient unit

27 Second coefficient unit
28 Selector
29 Adder
30 D flip-flop
34 Smoothing unit
36 Amount-of-time-shift calculating unit
37 Adder

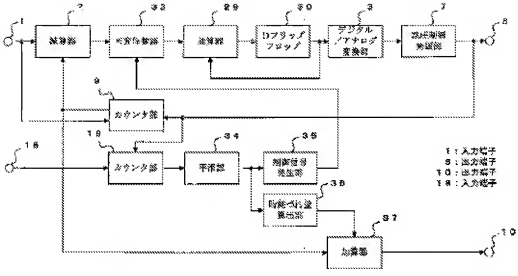


Figure 9

Legend: 1: Input terminal
8: Output terminal
10: Output terminal
18: Input terminal

Key: 2 Subtractor
3 Digital/analog converting unit
7 Voltage-controlled oscillation unit
9 Counter unit
19 Counter unit
29 Adder
30 D flip-flop
33 Variable coefficient unit
34 Smoothing unit
35 Control signal generating unit
36 Amount-of-time-shift calculating unit
37 Adder

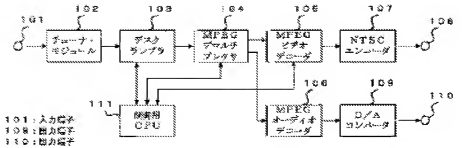


Figure 10

Legend: 101: Input terminal
108: Output terminal
110: Output terminal

Key: 102 Tuner module
103 Descrambler
104 MPEG demultiplexer
105 MPEG video decoder
106 MPEG audio decoder
107 NTSC encoder
109 D/A converter
111 Control CPU

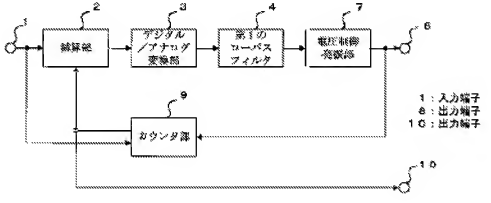


Figure 11

Legend: 1: Input terminal
8: Output terminal
10 Output unit

Key: 2 Subtracting unit
3 Digital/analog converting unit
4 First low pass filter
7 Voltage-controlled oscillation unit
9 Counter unit

Continuation of front page

F Terms (reference)

5J106 AA04 BB02 BB04 CC01 CC26
CC38 CC41 CC52 DD09 DD19
DD36 DD44 EE10 FF02 GG07
HH10 JJ09 KK05 KK25 LL07
5K047 AA06 CC08 GG09 GG45 MM33
MM35 MM46 MM50 MM58 MM63